PATENT ABSTRACTS OF JAPAN

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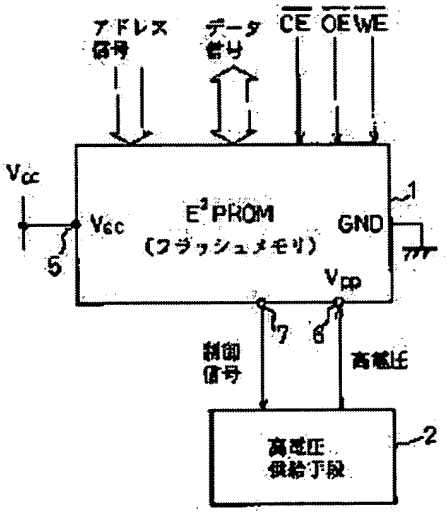
(54) NON-VOLATILE SEMICONDUCTOR MEMORY

(57)Abstract:

PURPOSE: To enable using an EEPROM such as a flash memory and the like requiring two power supplies with the same operation as that of a EEPROM having one power supply by providing a high voltage control signal terminal which outputs a control signal controlling whether high voltage is to be applied to a high voltage supplying device or not.



CONSTITUTION: This non-volatile semiconductor memory requires higher power supply voltage Vpp than power supply voltage Vcc used in reading out at the time of writing or erasing data. And this device is provided with a high voltage control signal terminal 7 which outputs a control signal controlling whether high voltage is to be supplied to a high voltage supplying device 2 or not, and outputs the control signal according to demand. Thereby, the device 2 is not required to control by a system side as performed conventionally, by accessing to the non-volatile semiconductor memory in the same way as a nonvolatile semiconductor memory of a single power supply, the non-volatile semiconductor device automatically control the device 2 according to demand. Therefore, this device may be operated with the same operation as that of a non-volatile device of a single power supply, software is not required to change.

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CLAIMS

[Claim(s)]
[Claim 1] At the time of the writing of data, or elimination, supply voltage (Vpp) higher than the supply voltage (Vcc) used at the time of read-out is needed. In a non-volatile semiconductor memory equipped with the power supply terminal for said high voltages (6) supplied from an external high voltage supply means (2) besides the terminal for standard power sources (5) The non-volatile semiconductor memory characterized by having the high-voltage control signal terminal (7) which outputs the control signal which controls whether the high voltage is made to supply to said high voltage supply means (2).
[Claim 2] It is the non-volatile semiconductor memory according to claim 1 characterized by having a command judging means (49) to judge whether it is the actuation which needs the high voltage from the command signal inputted into the non-volatile semiconductor memory concerned, for this command judging means (49) outputting said control signal which directs initiation of high voltage supply when the high voltage is a required command, and outputting said control signal which will direct a halt of high voltage supply if the high voltage is not required.
[Claim 3] The non-volatile semiconductor memory according to claim 1 or 2 characterized by starting the actuation which needs the high voltage from the time of having an electrical-potential-difference check means (48) to judge that the electrical-potential-difference value of the high voltage supplied is beyond a predetermined value, and the high voltage supplied becoming beyond a predetermined value.
[Claim 4] Claims 1 and 2 characterized by having a delay means (72) to make the actuation which needs the high voltage start after predetermined time progress from loss sending out of a control signal which directs initiation of said high voltage, or a non-volatile semiconductor memory given in either of 3.
[Claim 5] At the time of the writing of data, or elimination, supply voltage (Vpp) higher than the supply voltage (Vcc) used at the time of read-out is needed. In the non-volatile semiconductor memory which contains the switching circuit (103) for pressure ups which supplies this high supply voltage (Vpp) It has a command judging means (49) to judge whether it is the actuation which needs the high voltage from the command signal inputted into the non-volatile semiconductor memory concerned. This command judging means (49) is a non-volatile semiconductor memory characterized by outputting said control signal which directs initiation of high voltage supply when it is the command which needs the high voltage, and outputting said control signal which will direct a halt of high voltage supply if the high voltage is not required.
[Claim 6] The passive component which constitutes said switching circuit (103) for pressure ups is a non-volatile semiconductor memory according to claim 5 characterized by being attached from the exterior of the non-volatile semiconductor memory concerned.
[Claim 7] Said passive component by which external is carried out is a non-volatile semiconductor memory according to claim 6 characterized by being an inductance component.
[Claim 8] Said passive component by which external is carried out is a non-volatile semiconductor memory according to claim 6 characterized by being a capacitative element.
[Claim 9] The non-volatile semiconductor memory according to claim 5 to 8 characterized by starting the actuation which needs the high voltage from the time of having an electrical-potential-difference

check means (48) to judge that the electrical-potential-difference value of the high voltage supplied is beyond a predetermined value, and the high voltage supplied becoming beyond a predetermined value.
[Claim 10] The non-volatile semiconductor memory according to claim 5 to 8 characterized by having a delay means (72) to make the actuation which needs the high voltage start after predetermined time progress from loss sending out of a control signal which directs initiation of said high voltage.
[Claim 11] The non-volatile semiconductor memory according to claim 6 to 10 characterized by closing a non-volatile semiconductor memory and said passive component by which external is carried out concerned in the same package.
[Claim 12] The computer system which has the non-volatile semiconductor memory characterized by having a non-volatile semiconductor memory as a part of storage means, and having the control means which generates the control signal of said switching circuit for pressure ups automatically according to the access actuation to said non-volatile semiconductor memory in a computer system equipped also with the switching circuit for pressure ups which generates the high voltage needed at the time of the writing of this non-volatile semiconductor memory, or elimination.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to EEPROM (Electrically Erasable Programable Read Only Memory) which can eliminate stored data electrically especially about the non-volatile semiconductor memory which needs supply voltage higher than the supply voltage used at the time of read-out at the time of writing or elimination. The flash memory which is the whole equipment, or bundles up elimination for every block and performs it is a kind of this EEPROM.
[0002]
[Description of the Prior Art] In recent years, the non-volatile semiconductor memory which can eliminate stored data electrically, and the so-called EEPROM attract attention, and since a flash memory can be integrated highly also in it, it is observed as what replaces magnetic storage. Although hereafter explained by making a flash memory into an example, this invention is applicable also to the usual EEPROM.
[0003] A flash memory has the dual structure of the floating gate and the control gate, and information is memorized by whether there is any paddle with which the charge is accumulated in the floating gate. As for writing, it is common by impressing the about [+12V] high voltage to the control gate, impressing an about [+6V] electrical potential difference to a drain, and grounding the source to carry out by pouring a hot electron into the floating gate. At the time of read-out, an about [+5V] electrical potential difference is impressed to the control gate, an about [+1V] electrical potential difference is impressed to a drain, the source is grounded, and it carries out by detecting the current difference which changes with existence of the charge storage in the floating gate. At the time of elimination, the about [+12V] high voltage is impressed to the source, the control gate is grounded, a drain is opened wide, the tunnel current between bands is generated, and an electron is drawn out in the source from the floating gate. At the time of writing, an about several mA current flows as a drain current, and, on the whole, an about dozens of mA current flows. Therefore, the high-voltage power source which outputs not only the standard power source of an electrical potential difference Vcc (+5V) but the high voltage Vpp (+12V) is needed.
[0004] Drawing 11 is the computer system which has a flash memory, and shows the conventional configuration when preparing the source of high voltage supply in addition to a standard power source. As for a central processing unit (CPU) and 112, in drawing, 111 is [ROM/RAM and 113] control ports, as for a flash memory and 118, for the source of high voltage supply to control the source 118 of high voltage supply, and for a system control 119 in an input/output port (I/O) port and 114, as for a peripheral device and 115. The source 118 of high voltage supply consists of a high-voltage control circuit 116 and the high-voltage generating section 117, and it is controlled by control from CPU111 through a control port 119 whether the high voltage Vpp is supplied to a flash memory 115 or it does not carry out. As for a booster circuit, the high-voltage generating section 117 may also be the case of a fixed power source. If it is a fixed power source, the high-voltage control circuit 116 is a mere transfer switch. If it is a booster circuit, a circuit can be started now if needed for power consumption reduction,

and the high-voltage control circuit 116 will turn into the control circuit.
[0005] In the computer system which used the flash memory, writing or elimination is not frequently performed to a flash memory, and the high voltage is supplied if needed. Drawing 12 is a flow chart which shows control of the source of the high voltage at the time of store/elimination actuation in the computer system of drawing 11 . According to drawing, actuation is explained briefly. At step 1201, the signal which directs supply of the high voltage to the source control port 119 of the high voltage is outputted. Thereby, if it is a fixed power source, the high-voltage control circuit 116 will be switched to the side which supplies the high voltage. A pressure up will be started if it is a booster circuit.
[0006] At step 1202, standby actuation until sufficient high voltage is supplied is performed. This step is unnecessary if it is a fixed power source. At step 1203, the writing or elimination command to a flash memory is written in. Step 1204 and step 1205 are parts which check the condition after step 1203, and if satisfactory, they will output the signal which directs the supply interruption of the high voltage through the source control port 119 of the high voltage at step 1203. Supply of the high voltage is suspended according to this.
[0007] Although it is the conventional processing actuation when the above prepares the source of high voltage supply in addition to a standard power source, the flash memory which can be preferably used by the single power supply is demanded on use that it is necessary to prepare such a source of the high voltage independently. In order to enable it to use it by the single power supply, in the current flash memory, single power supply-ization is attained by establishing the electrical potential difference Vcc of a standard power source in the interior, and establishing a booster circuit in the high voltage Vpp. In that case, this high voltage Vpp that carried out the pressure up is impressed to the control gate, and the electrical potential difference Vcc of the standard power source instead of +6V is impressed to a drain. If it is this, the avalanche breakdown voltage of a drain will fall, but since a current hardly flows in the control gate, electrical-potential-difference impression is made [at it] by it even in the small internal booster circuit of current serviceability. Since a standard power source can be used, writing and elimination can be performed in electrical-potential-difference impression to the drain with which the amount of currents becomes large by the single power supply.
[0008]
[Problem(s) to be Solved by the Invention] However, low-battery-ization of a standard power source is also attained for low-power-izing of a flash memory etc., and the situation that the electrical potential difference Vcc of the standard power source impressed to a drain becomes lower than the electrical potential difference which causes avalanche breakdown has arisen by the approach of impressing the electrical potential difference Vcc of a standard power source to the above-mentioned drain directly. Therefore, the problem of it becoming impossible to use an approach to write in the above has occurred.
[0009] Then, although it is possible to prepare the source of the high voltage independently as before, when using the flash memory which needs the source of the high voltage for such a system independently, modification of the software which controls the source of the high voltage is needed [many systems are already made on the assumption that the above-mentioned single-power-supply-izing, and]. However, such modification has the problem of it being complicated and reducing the value as a product of a flash memory remarkably.
[0010] Moreover, by the low battery, since it cannot be used, it is necessary to set up highly the electrical potential difference Vcc of a standard power source, and there is a problem that low-battery-ization of a standard power source cannot be performed. Although this invention is made in view of the above-mentioned trouble and two power sources are used for it, it aims at implementation of the easy non-volatile semiconductor memory of the operation which can be substantially used by the same actuation as a single power supply.
[0011]
[Means for Solving the Problem] Drawing 1 is the principle explanatory view of the non-volatile semiconductor memory in which electric elimination of this invention is possible. Like illustration, the non-volatile semiconductor memory of this invention At the time of the writing of data, or elimination, the supply voltage Vpp higher than the supply voltage Vcc used at the time of read-out is needed. In

order to be a non-volatile semiconductor memory equipped with the power supply terminal 6 for high voltages supplied from the external high voltage supply means 2 besides the terminal for standard power sources and to realize the above-mentioned purpose, It is characterized by having the high-voltage control signal terminal 7 which outputs the control signal which controls whether the high voltage is made to supply to the high voltage supply means 2.

[0012] furthermore, the second voice of this invention -- it is characterized by to equip a non-volatile semiconductor memory [like] with a command judging means judge whether it is the actuation which needs the high voltage, from the command signal inputted into the non-volatile semiconductor memory itself, for this command judging means to output the control signal which directs initiation of high voltage supply, when it is the command which needs the high voltage, and to output the control signal which will direct a halt of high voltage supply if the high voltage is not required.

[0013]

[Function] The non-volatile semiconductor memory (EEPROM) of this invention equips the high voltage supply means 2 with the high-voltage control signal terminal 7 which outputs the control signal which controls whether the high voltage is made to supply, and outputs a control signal if needed. Therefore, it is not necessary to control the high voltage supply means 2 from a system side like before, and like the case where it is the non-volatile semiconductor memory of a single power supply, if a non-volatile semiconductor memory is accessed, a non-volatile semiconductor memory will control the high voltage supply means 2 automatically if needed. Therefore, modification of software etc. is [that what is necessary is just to perform the same actuation as the non-volatile semiconductor memory of a single power supply] unnecessary.

[0014] Drawing 2 is a flow chart which shows the procedure when performing actuation which needs the high voltage in the system which used the non-volatile semiconductor memory (EEPROM) of this invention. Left-hand side steps 201-204 show the processing by the side of a system, and right-hand side steps 210-213 show processing of EEPROM. At step 201, writing/elimination command is sent out to EEPROM. According to this, EEPROM is step 210 and judges whether it is writing/elimination command. If it is read-out actuation, since the high voltage is unnecessary, read-out actuation is performed without performing the following processings. If it is writing/elimination actuation, the directions which start the output of the high voltage from the high-voltage control signal terminal 7 are sent out at step 211. Then, it stands by until the electrical-potential-difference value of the high voltage supplied turns into sufficient value, but as mentioned above, if a high-voltage power source is a fixed power source, standby actuation is unnecessary.

[0015] After the electrical-potential-difference value of the high voltage turns into sufficient value, writing/elimination actuation is performed at step 212. In elimination actuation, a system side needs to perform no actuation, and carries out another processing to it. If it is write-in actuation, a system side writes in and data are sent out. make it any -- a system side performs check actuation at the termination-in the middle of writing/elimination actuation time. This is steps 202 and 203.

[0016] At step 204, the signal which notifies that writing/elimination actuation to EEPROM was completed is sent out. According to this, EEPROM sends out the signal which directs the supply interruption of the high voltage at step 213. to some extent [since writing/elimination actuation is performed by usually gathering a lot of data / writing/elimination actuation] -- it is carried out by carrying out time amount continuation. Therefore, when it detects that a certain amount of time amount writing / elimination actuation was not performed, you may make it EEPROM send out the signal which directs the supply interruption of the high voltage automatically.

[0017] Anyway, the processing by the side of a system becomes easy compared with the conventional example shown in drawing 12 R> 2.

[0018]

[Example] Drawing 3 is drawing showing the whole example configuration of this invention. In drawing, 31 is a central processing unit (CPU) and a DC-DC converter with which in an I/O Port and 34 a peripheral device and 35 generate the flash memory of this invention, and 36 generates [32 / ROM/RAM and 33] the high voltage. As for DC-DC converter 36, starting and a halt are controlled by

the control signal from a flash memory 35.
[0019] As compared with drawing 11 , there is no output port for CPU to control DC-DC converter 36 so that clearly. The configuration of drawing 3 is the same as the case where the flash memory of a single power supply is used. Drawing 4 is drawing showing the internal configuration of the flash memory of drawing 3 . Like illustration, this flash memory has an address buffer 41, the line decoder 42, the train decoder 43, memory cell MARIKUSU 44, read-out / write-in amplifier 45, the input output buffer 46, and the control section 47, and has an address terminal, the data terminal, the standard power-source (Vcc) terminal, the high-voltage (Vpp) terminal, and the control terminal as an external I/O terminal. These are the same as the conventional flash memory.
[0020] Differing from the conventional flash memory are the command judging section 49, the point of having the electrical-potential-difference check circuit 48, and the point of having a source control terminal of the high voltage as an external I/O terminal. The command judging section 49 is a comparator circuit which detects coincidence with the command code of writing/elimination actuation to a flash memory, and when CPU31 outputs writing/elimination command to a flash memory, it outputs the signal which detects this and directs supply initiation of the high voltage for the source control terminal of the high voltage. Moreover, the timer circuit reset by write-in signal *WE is sufficient.
[0021] The electrical-potential-difference check circuit 48 is a circuit which detects whether the high voltage supplied has an electrical-potential-difference value more than predetermined, for example, is a circuit as shown in drawing 6 . In addition, the circuit of drawing 6 judges whether the high voltage Vpp impressed not only to the high voltage but to an internal electrical power source line and standard voltage Vcc are beyond each predetermined value. In drawing 6 , 61 is the body part of a control section and is a sequential circuit which performs processing which is mentioned later. 62 is a comparator and compares with two kinds of reference voltages r1 and r2 the electrical potential difference which pressured partially the electrical potential difference impressed to the internal electrical power source line 64 by resistance 65. The reference voltage to compare is switched with a switch 63.
[0022] Drawing 5 shows the external power control action in the flash memory of this example. At step 501, the signal outputted to a flash memory from CPU is investigated, and it is judged whether the high voltage is required. If the high voltage is required, the seizing signal to DC-DC converter 36 is sent out at step 502. It takes a certain amount of time amount for a DC-DC converter to output an electrical potential difference predetermined [after starting]. Then, at step 502, the electrical-potential-difference check circuit 50 stands by until it detects that the electrical potential difference of an internal electrical power source line is beyond a predetermined value.
[0023] When an electrical potential difference becomes beyond a predetermined value, the writing or elimination actuation of step 504 is performed. This actuation is performed continuously. After all writing or elimination actuation are completed, at step 505, in writing, it checks and it is checked [whether data are written in correctly and] whether in elimination, it is eliminated correctly. Although the stop signal to DC-DC converter 36 is sent out at step 506 if satisfactory, an internal electrical power source is switched to coincidence. According to this, DC-DC converter 36 stops a pressure up.
[0024] At step 507, it is checked that the switched internal electrical power source has returned to the usual electrical potential difference, and it ends. As long as it measures beforehand time amount until it reaches the predetermined electrical potential difference after starting, you may make it start the actuation which needs the high voltage after this time amount progress, although the electrical potential difference outputted from DC-DC converter 36 using the electrical-potential-difference check circuit of drawing 6 was checked in processing actuation of drawing 5 R> 5. Drawing 7 is an example of a circuit for it.
[0025] If it checks that it is the actuation which needs the high voltage, the control-section body 71 will output the signal which starts a DC-DC converter to a high-voltage-power-supply control terminal, and will suspend actuation temporarily. This seizing signal is inputted also into a delay circuit 72, and a delay circuit 72 sends out a delay signal to the after [predetermined time of] control-section body 71. According to this, the control-section body 71 resumes actuation.
[0026] Although the control action of drawing 5 is realizable even if it naturally uses a microcomputer,

it is not realistic to build a microcomputer into a flash memory, and it has realized the control circuit here combining an above-mentioned delay circuit and an above-mentioned logical circuit. Although DC-DC converter 36 was formed in the exterior of a flash memory 35 in the above-mentioned example, the controlling mechanism which could also build the DC-DC converter into the flash memory, and explained it even in such a case until now is useful. A DC-DC converter is explained here.

[0027] Drawing 8 and 9 are drawings showing the basic configuration of a DC-DC converter circuit. Drawing 8 is the example which used the inductance component. In drawing, 82 is an oscillator circuit and 83 is a switch for controlling pressure-up actuation. 84 is a switch turned on and off by the signal from an oscillator circuit 82, 85 is diode, and 86 is a coil at the inductance component and concrete target which were connected between a standard power source and diode 85. When a switch 84 is turned on and off, the voltage swing of the input edge of diode 85 increases by the same principle as a transformer, by diode 85, only a high-voltage component flows into an outgoing end, and a pressure up is performed. By switching a switch 83, it is controlled whether a switch 84 is turned on and off, and control of a pressure up is performed. Here, although parts other than coil 86 can be made comparatively small and it can include in a flash memory, a coil 86 is seldom made into small in relation with the engine performance. Therefore, when building a DC-DC converter into a flash memory, it is desirable to attach only a coil 86 from the exterior of a flash memory.

[0028] Drawing 9 is drawing showing the basic configuration of the DC-DC converter circuit which used the capacitative element (capacitor) as a passive component, and although detailed explanation is omitted, control of a pressure up is performed by whether an oscillator 92 is operated or it does not carry out. ** which includes a capacitative element 94 in a flash memory also in the circuit of drawing 9 -- since it is difficult, it is desirable to attach only a capacitative element 94 from the exterior of a flash memory.

[0029] Drawing 10 attaches the passive components 104, such as the above-mentioned inductance component and a capacitative element, in the component which combined the flash memory 102 and DC-DC converter 103, and holds them in it at the package of a piece.

[0030]

[Effect of the Invention] By this invention, EEPROMs, such as a flash memory which needs two power sources, can use it now by the same actuation as EEPROM of one power source. Moreover, since it becomes unnecessary to include the booster circuit for power sources in a flash memory by this, low supply voltage-ization of the flash memory itself is also attained.

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TECHNICAL FIELD

[Industrial Application] This invention relates to EEPROM (Electrically Erasable Programable Read Only Memory) which can eliminate stored data electrically especially about the non-volatile semiconductor memory which needs supply voltage higher than the supply voltage used at the time of read-out at the time of writing or elimination. The flash memory which is the whole equipment, or bundles up elimination for every block and performs it is a kind of this EEPROM.

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PRIOR ART

[Description of the Prior Art] In recent years, the non-volatile semiconductor memory which can eliminate stored data electrically, and the so-called EEPROM attract attention, and since a flash memory can be integrated highly also in it, it is observed as what replaces magnetic storage. Although hereafter explained by making a flash memory into an example, this invention is applicable also to the usual EEPROM.
[0003] A flash memory has the dual structure of the floating gate and the control gate, and information is memorized by whether there is any paddle with which the charge is accumulated in the floating gate. As for writing, it is common by impressing the about [+12V] high voltage to the control gate, impressing an about [+6V] electrical potential difference to a drain, and grounding the source to carry out by pouring a hot electron into the floating gate. At the time of read-out, an about [+5V] electrical potential difference is impressed to the control gate, an about [+1V] electrical potential difference is impressed to a drain, the source is grounded, and it carries out by detecting the current difference which changes with existence of the charge storage in the floating gate. At the time of elimination, the about [+12V] high voltage is impressed to the source, the control gate is grounded, a drain is opened wide, the tunnel current between bands is generated, and an electron is drawn out in the source from the floating gate. At the time of writing, an about several mA current flows as a drain current, and, on the whole, an about dozens of mA current flows. Therefore, the high-voltage power source which outputs not only the standard power source of an electrical potential difference Vcc (+5V) but the high voltage Vpp (+12V) is needed.
[0004] Drawing 11 is the computer system which has a flash memory, and shows the conventional configuration when preparing the source of high voltage supply in addition to a standard power source. As for a central processing unit (CPU) and 112, in drawing, 111 is [ROM/RAM and 113] control ports, as for a flash memory and 118, for the source of high voltage supply to control the source 118 of high voltage supply, and for a system control 119 in an input/output port (I/O) port and 114, as for a peripheral device and 115. The source 118 of high voltage supply consists of a high-voltage control circuit 116 and the high-voltage generating section 117, and it is controlled by control from CPU111 through a control port 119 whether the high voltage Vpp is supplied to a flash memory 115 or it does not carry out. As for a booster circuit, the high-voltage generating section 117 may also be the case of a fixed power source. If it is a fixed power source, the high-voltage control circuit 116 is a mere transfer switch. If it is a booster circuit, a circuit can be started now if needed for power consumption reduction, and the high-voltage control circuit 116 will turn into the control circuit.
[0005] In the computer system which used the flash memory, writing or elimination is not frequently performed to a flash memory, and the high voltage is supplied if needed. Drawing 12 is a flow chart which shows control of the source of the high voltage at the time of store/elimination actuation in the computer system of drawing 11 . According to drawing, actuation is explained briefly. At step 1201, the signal which directs supply of the high voltage to the source control port 119 of the high voltage is outputted. Thereby, if it is a fixed power source, the high-voltage control circuit 116 will be switched to the side which supplies the high voltage. A pressure up will be started if it is a booster circuit.

[0006] At step 1202, standby actuation until sufficient high voltage is supplied is performed. This step is unnecessary if it is a fixed power source. At step 1203, the writing or elimination command to a flash memory is written in. Step 1204 and step 1205 are parts which check the condition after step 1203, and if satisfactory, they will output the signal which directs the supply interruption of the high voltage through the source control port 119 of the high voltage at step 1203. Supply of the high voltage is suspended according to this.

[0007] Although it is the conventional processing actuation when the above prepares the source of high voltage supply in addition to a standard power source, the flash memory which can be preferably used by the single power supply is demanded on use that it is necessary to prepare such a source of the high voltage independently. In order to enable it to use it by the single power supply, in the current flash memory, single power supply-ization is attained by establishing the electrical potential difference Vcc of a standard power source in the interior, and establishing a booster circuit in the high voltage Vpp. In that case, this high voltage Vpp that carried out the pressure up is impressed to the control gate, and the electrical potential difference Vcc of the standard power source instead of +6V is impressed to a drain. If it is this, the avalanche breakdown voltage of a drain will fall, but since a current hardly flows in the control gate, electrical-potential-difference impression is made [at it] by it even in the small internal booster circuit of current serviceability. Since a standard power source can be used, writing and elimination can be performed in electrical-potential-difference impression to the drain with which the amount of currents becomes large by the single power supply.

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EFFECT OF THE INVENTION

[Effect of the Invention] By this invention, EEPROMs, such as a flash memory which needs two power sources, can use it now by the same actuation as EEPROM of one power source. Moreover, since it becomes unnecessary to include the booster circuit for power sources in a flash memory by this, low supply voltage-ization of the flash memory itself is also attained.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, low-battery-ization of a standard power source is also attained for low-power-izing of a flash memory etc., and the situation that the electrical potential difference Vcc of the standard power source impressed to a drain becomes lower than the electrical potential difference which causes avalanche breakdown has arisen by the approach of impressing the electrical potential difference Vcc of a standard power source to the above-mentioned drain directly. Therefore, the problem of it becoming impossible to use an approach to write in the above has occurred.
[0009] Then, although it is possible to prepare the source of the high voltage independently as before, when using the flash memory which needs the source of the high voltage for such a system independently, modification of the software which controls the source of the high voltage is needed [many systems are already made on the assumption that the above-mentioned single-power-supply-izing, and]. However, such modification has the problem of it being complicated and reducing the value as a product of a flash memory remarkably.
[0010] Moreover, by the low battery, since it cannot be used, it is necessary to set up highly the electrical potential difference Vcc of a standard power source, and there is a problem that low-battery-ization of a standard power source cannot be performed. Although this invention is made in view of the above-mentioned trouble and two power sources are used for it, it aims at implementation of the easy non-volatile semiconductor memory of the operation which can be substantially used by the same actuation as a single power supply.

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MEANS

[Means for Solving the Problem] Drawing 1 is the principle explanatory view of the non-volatile semiconductor memory in which electric elimination of this invention is possible. Like illustration, the non-volatile semiconductor memory of this invention At the time of the writing of data, or elimination, the supply voltage Vpp higher than the supply voltage Vcc used at the time of read-out is needed. In order to be a non-volatile semiconductor memory equipped with the power supply terminal 6 for high voltages supplied from the external high voltage supply means 2 besides the terminal for standard power sources and to realize the above-mentioned purpose, It is characterized by having the high-voltage control signal terminal 7 which outputs the control signal which controls whether the high voltage is made to supply to the high voltage supply means 2.
[0012] furthermore, the second voice of this invention -- it is characterized by to equip a non-volatile semiconductor memory [like] with a command judging means judge whether it is the actuation which needs the high voltage, from the command signal inputted into the non-volatile semiconductor memory itself, for this command judging means to output the control signal which directs initiation of high voltage supply, when it is the command which needs the high voltage, and to output the control signal which will direct a halt of high voltage supply if the high voltage is not required.

[Translation done.]

* NOTICES *

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OPERATION

[Function] The non-volatile semiconductor memory (EEPROM) of this invention equips the high voltage supply means 2 with the high-voltage control signal terminal 7 which outputs the control signal which controls whether the high voltage is made to supply, and outputs a control signal if needed. Therefore, it is not necessary to control the high voltage supply means 2 from a system side like before, and like the case where it is the non-volatile semiconductor memory of a single power supply, if a non-volatile semiconductor memory is accessed, a non-volatile semiconductor memory will control the high voltage supply means 2 automatically if needed. Therefore, modification of software etc. is [that what is necessary is just to perform the same actuation as the non-volatile semiconductor memory of a single power supply] unnecessary.
[0014] Drawing 2 is a flow chart which shows the procedure when performing actuation which needs the high voltage in the system which used the non-volatile semiconductor memory (EEPROM) of this invention. Left-hand side steps 201-204 show the processing by the side of a system, and right-hand side steps 210-213 show processing of EEPROM. At step 201, writing/elimination command is sent out to EEPROM. According to this, EEPROM is step 210 and judges whether it is writing/elimination command. If it is read-out actuation, since the high voltage is unnecessary, read-out actuation is performed without performing the following processings. If it is writing/elimination actuation, the directions which start the output of the high voltage from the high-voltage control signal terminal 7 are sent out at step 211. Then, it stands by until the electrical-potential-difference value of the high voltage supplied turns into sufficient value, but as mentioned above, if a high-voltage power source is a fixed power source, standby actuation is unnecessary.
[0015] After the electrical-potential-difference value of the high voltage turns into sufficient value, writing/elimination actuation is performed at step 212. In elimination actuation, a system side needs to perform no actuation, and carries out another processing to it. If it is write-in actuation, a system side writes in and data are sent out. make it any -- a system side performs check actuation at the termination-in the middle of writing/elimination actuation time. This is steps 202 and 203.
[0016] At step 204, the signal which notifies that writing/elimination actuation to EEPROM was completed is sent out. According to this, EEPROM sends out the signal which directs the supply interruption of the high voltage at step 213. to some extent [since writing/elimination actuation is performed by usually gathering a lot of data / writing/elimination actuation] -- it is carried out by carrying out time amount continuation. Therefore, when it detects that a certain amount of time amount writing / elimination actuation was not performed, you may make it EEPROM send out the signal which directs the supply interruption of the high voltage automatically.
[0017] Anyway, the processing by the side of a system becomes easy compared with the conventional example shown in drawing 12 R> 2.

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EXAMPLE

[Example] Drawing 3 is drawing showing the whole example configuration of this invention. In drawing, 31 is a central processing unit (CPU) and a DC-DC converter with which in an I/O Port and 34 a peripheral device and 35 generate the flash memory of this invention, and 36 generates [32 / ROM/RAM and 33] the high voltage. As for DC-DC converter 36, starting and a halt are controlled by the control signal from a flash memory 35.
[0019] As compared with drawing 11 , there is no output port for CPU to control DC-DC converter 36 so that clearly. The configuration of drawing 3 is the same as the case where the flash memory of a single power supply is used. Drawing 4 is drawing showing the internal configuration of the flash memory of drawing 3 . Like illustration, this flash memory has an address buffer 41, the line decoder 42, the train decoder 43, memory cell MARIKUSU 44, read-out / write-in amplifier 45, the input output buffer 46, and the control section 47, and has an address terminal, the data terminal, the standard power-source (Vcc) terminal, the high-voltage (Vpp) terminal, and the control terminal as an external I/O terminal. These are the same as the conventional flash memory.
[0020] Differing from the conventional flash memory are the command judging section 49, the point of having the electrical-potential-difference check circuit 48, and the point of having a source control terminal of the high voltage as an external I/O terminal. The command judging section 49 is a comparator circuit which detects coincidence with the command code of writing/elimination actuation to a flash memory, and when CPU31 outputs writing/elimination command to a flash memory, it outputs the signal which detects this and directs supply initiation of the high voltage for the source control terminal of the high voltage. Moreover, the timer circuit reset by write-in signal *WE is sufficient.
[0021] The electrical-potential-difference check circuit 48 is a circuit which detects whether the high voltage supplied has an electrical-potential-difference value more than predetermined, for example, is a circuit as shown in drawing 6 . In addition, the circuit of drawing 6 judges whether the high voltage Vpp impressed not only to the high voltage but to an internal electrical power source line and standard voltage Vcc are beyond each predetermined value. In drawing 6 , 61 is the body part of a control section and is a sequential circuit which performs processing which is mentioned later. 62 is a comparator and compares with two kinds of reference voltages r1 and r2 the electrical potential difference which pressured partially the electrical potential difference impressed to the internal electrical power source line 64 by resistance 65. The reference voltage to compare is switched with a switch 63.
[0022] Drawing 5 shows the external power control action in the flash memory of this example. At step 501, the signal outputted to a flash memory from CPU is investigated, and it is judged whether the high voltage is required. If the high voltage is required, the seizing signal to DC-DC converter 36 is sent out at step 502. It takes a certain amount of time amount for a DC-DC converter to output an electrical potential difference predetermined [after starting]. Then, at step 502, the electrical-potential-difference check circuit 50 stands by until it detects that the electrical potential difference of an internal electrical power source line is beyond a predetermined value.
[0023] When an electrical potential difference becomes beyond a predetermined value, the writing or elimination actuation of step 504 is performed. This actuation is performed continuously. After all

writing or elimination actuation are completed, at step 505, in writing, it checks and it is checked [whether data are written in correctly and] whether in elimination, it is eliminated correctly. Although the stop signal to DC-DC converter 36 is sent out at step 506 if satisfactory, an internal electrical power source is switched to coincidence. According to this, DC-DC converter 36 stops a pressure up.

[0024] At step 507, it is checked that the switched internal electrical power source has returned to the usual electrical potential difference, and it ends. As long as it measures beforehand time amount until it reaches the predetermined electrical potential difference after starting, you may make it start the actuation which needs the high voltage after this time amount progress, although the electrical potential difference outputted from DC-DC converter 36 using the electrical-potential-difference check circuit of drawing 6 was checked in processing actuation of drawing 5 R> 5. Drawing 7 is an example of a circuit for it.

[0025] If it checks that it is the actuation which needs the high voltage, the control-section body 71 will output the signal which starts a DC-DC converter to a high-voltage-power-supply control terminal, and will suspend actuation temporarily. This seizing signal is inputted also into a delay circuit 72, and a delay circuit 72 sends out a delay signal to the after [predetermined time of] control-section body 71. According to this, the control-section body 71 resumes actuation.

[0026] Although the control action of drawing 5 is realizable even if it naturally uses a microcomputer, it is not realistic to build a microcomputer into a flash memory, and it has realized the control circuit here combining an above-mentioned delay circuit and an above-mentioned logical circuit. Although DC-DC converter 36 was formed in the exterior of a flash memory 35 in the above-mentioned example, the controlling mechanism which could also build the DC-DC converter into the flash memory, and explained it even in such a case until now is useful. A DC-DC converter is explained here.

[0027] Drawing 8 and 9 are drawings showing the basic configuration of a DC-DC converter circuit. Drawing 8 is the example which used the inductance component. In drawing, 82 is an oscillator circuit and 83 is a switch for controlling pressure-up actuation. 84 is a switch turned on and off by the signal from an oscillator circuit 82, 85 is diode, and 86 is a coil at the inductance component and concrete target which were connected between a standard power source and diode 85. When a switch 84 is turned on and off, the voltage swing of the input edge of diode 85 increases by the same principle as a transformer, by diode 85, only a high-voltage component flows into an outgoing end, and a pressure up is performed. By switching a switch 83, it is controlled whether a switch 84 is turned on and off, and control of a pressure up is performed. Here, although parts other than coil 86 can be made comparatively small and it can include in a flash memory, a coil 86 is seldom made into small in relation with the engine performance. Therefore, when building a DC-DC converter into a flash memory, it is desirable to attach only a coil 86 from the exterior of a flash memory.

[0028] Drawing 9 is drawing showing the basic configuration of the DC-DC converter circuit which used the capacitative element (capacitor) as a passive component, and although detailed explanation is omitted, control of a pressure up is performed by whether an oscillator 92 is operated or it does not carry out. ** which includes a capacitative element 94 in a flash memory also in the circuit of drawing 9 -- since it is difficult, it is desirable to attach only a capacitative element 94 from the exterior of a flash memory.

[0029] Drawing 10 attaches the passive components 104, such as the above-mentioned inductance component and a capacitative element, in the component which combined the flash memory 102 and DC-DC converter 103, and holds them in it at the package of a piece.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the principle explanatory view of the non-volatile semiconductor memory of this invention.
[Drawing 2] It is the flow chart which shows the procedure at the time of the actuation which needs the high voltage of the system using the non-volatile semiconductor memory (EEPROM) of this invention.
[Drawing 3] It is drawing showing the whole example configuration of this invention.
[Drawing 4] It is drawing showing the configuration of the flash memory in an example.
[Drawing 5] It is the flow chart which shows the control action in the flash memory of an example.
[Drawing 6] It is drawing showing the example of an electrical-potential-difference check circuit.
[Drawing 7] It is drawing showing the example of circuitry from which it moves to the next actuation by the predetermined time after control signal sending out.
[Drawing 8] It is drawing showing the first example of a circuit of a DC-DC converter.
[Drawing 9] It is drawing showing the second example of a circuit of a DC-DC converter.
[Drawing 10] It is drawing showing the example of a flash memory with a built-in DC-DC converter.
[Drawing 11] It is drawing showing the example of the structure of a system using the conventional flash memory.
[Drawing 12] It is the flow chart which shows the control action of the system using the conventional flash memory.
[Description of Notations]
1 -- Non-volatile semiconductor memory
2 -- High voltage supply means
5 -- Terminal for standard power sources
6 -- Power supply terminal for high voltages
7 -- High-voltage control signal terminal

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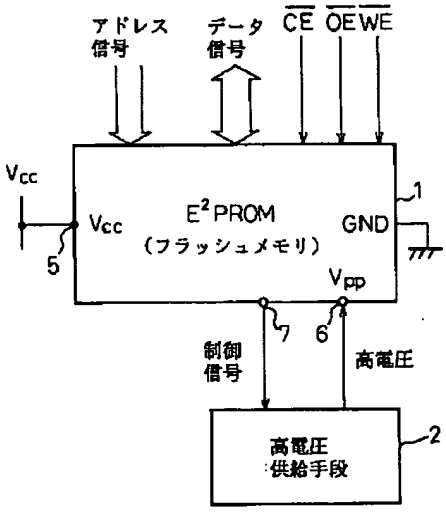
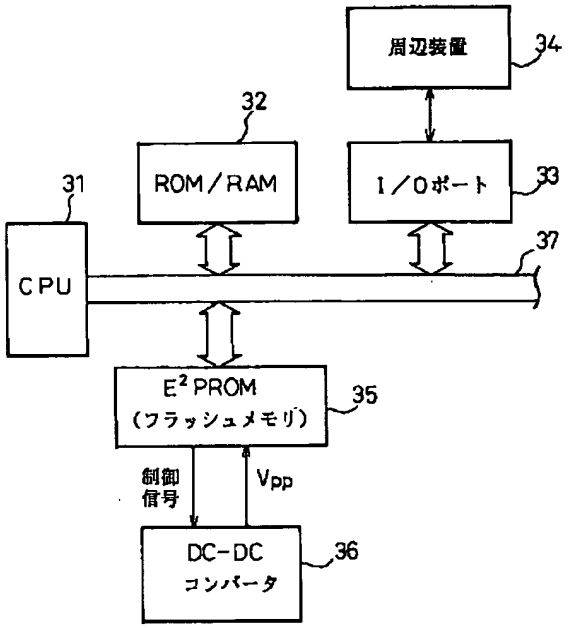
DRAWINGS

[Drawing 1]
本発明のE²PROMの原理説明図



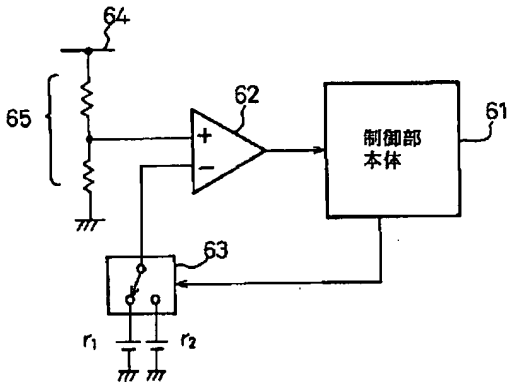
[Drawing 3]

実施例の全体構成



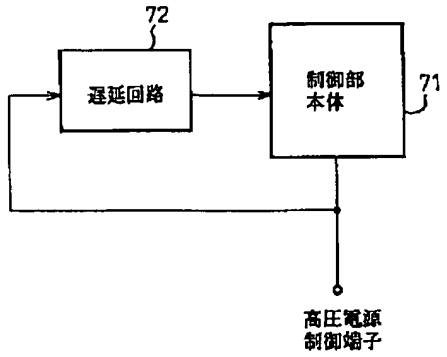
[Drawing 6]

電圧確認回路の例



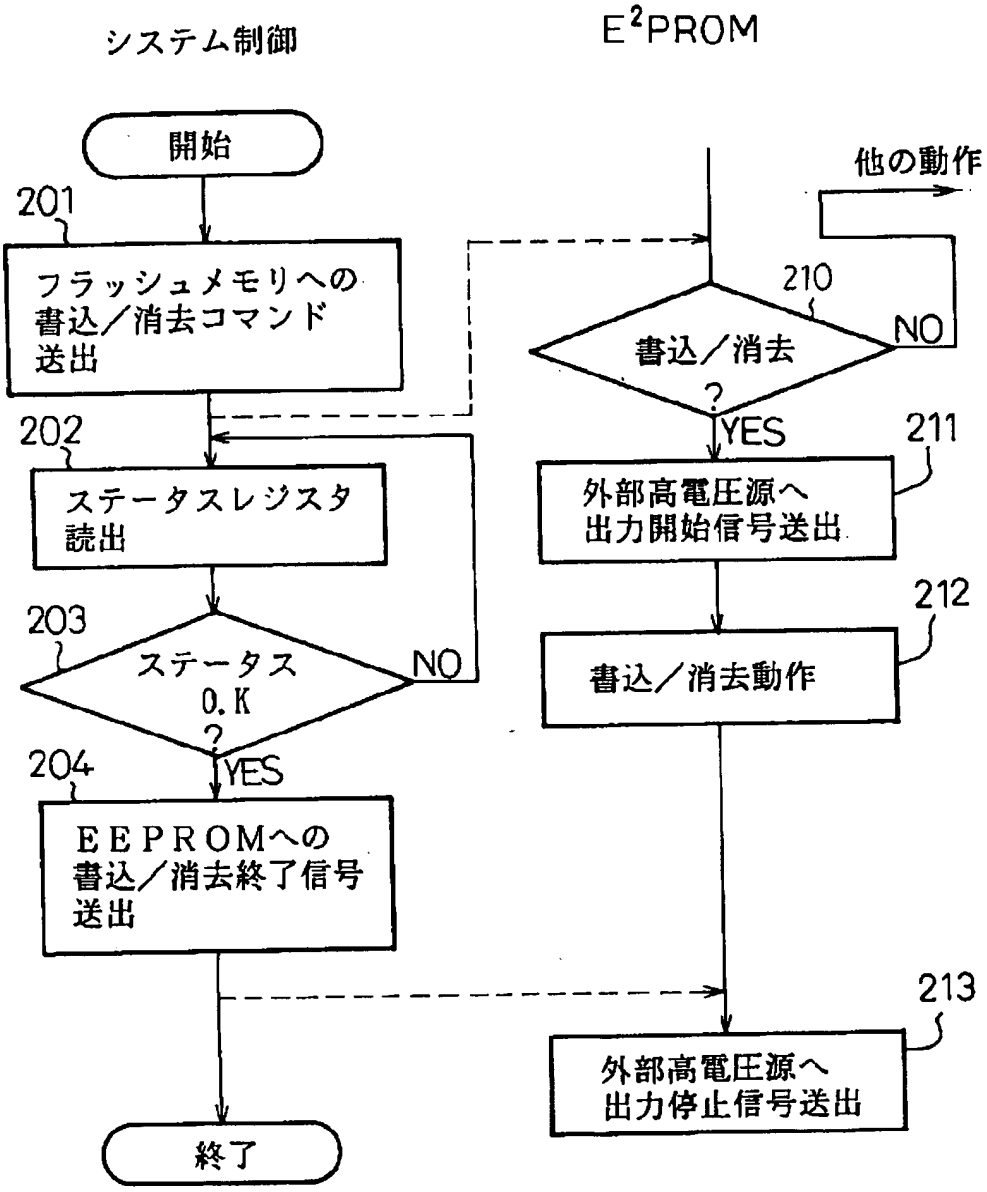
[Drawing 7]

制御信号送出後所定時間で次の動作へ移る例



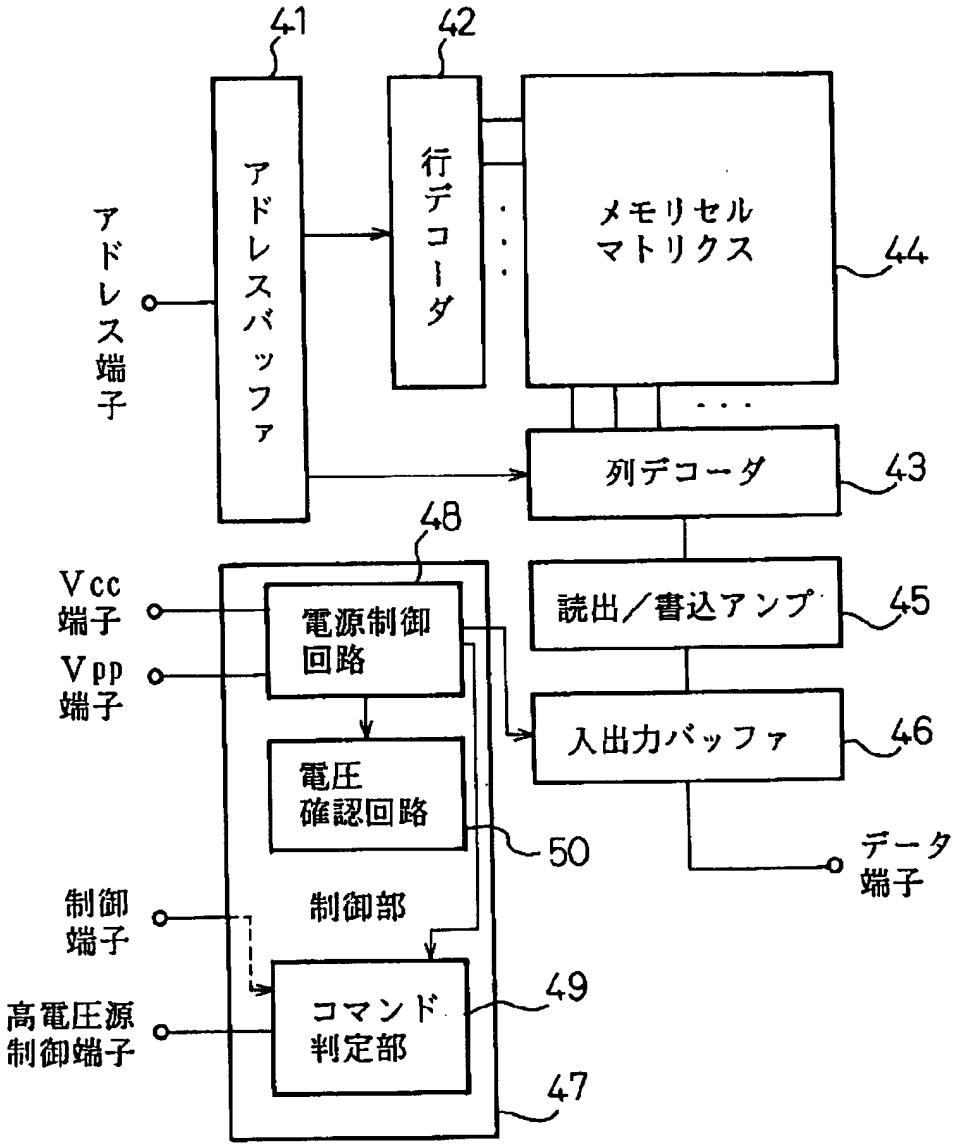
[Drawing 2]

本発明のE²PROMを用いたシステムの高電圧必要動作の処理手順



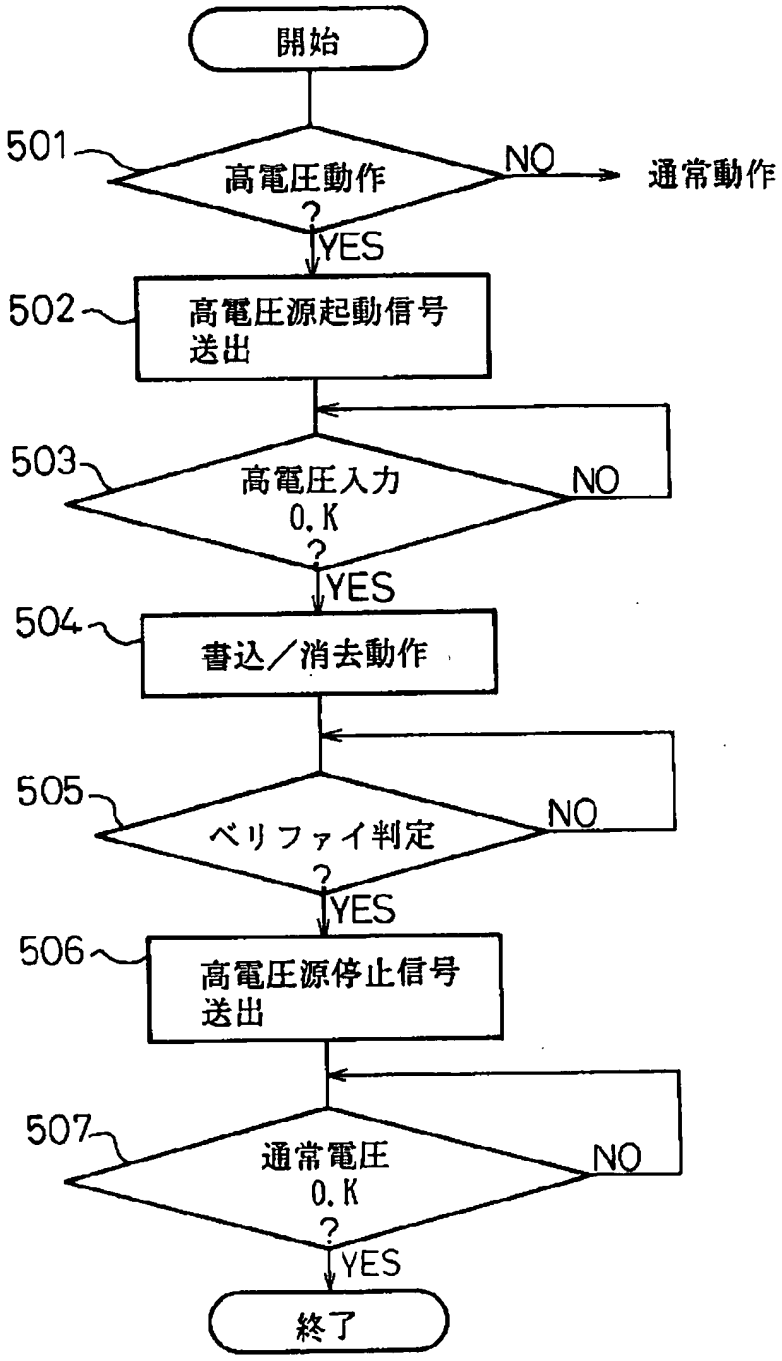
[Drawing 4]

実施例におけるフラッシュメモリの構成



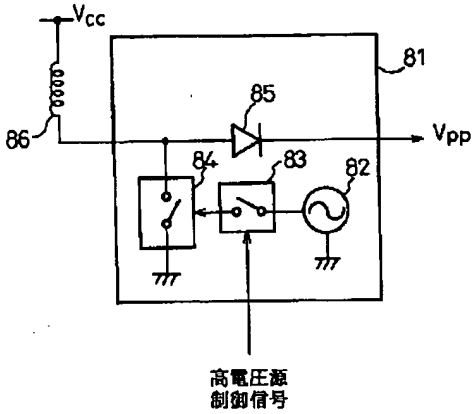
[Drawing 5]

実施例のフラッシュメモリおける制御動作



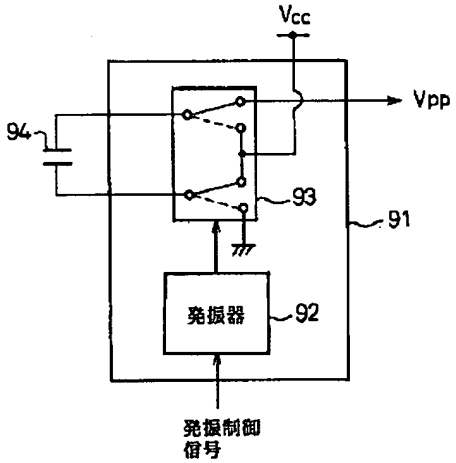
[Drawing 8]

DC－DCコンバータ回路例（その1）



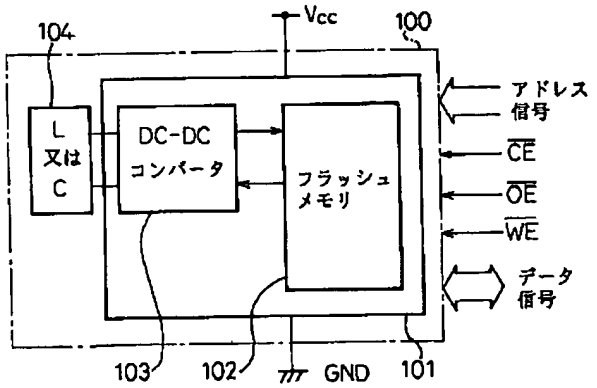
[Drawing 9]

DC－DCコンバータ回路例（その2）

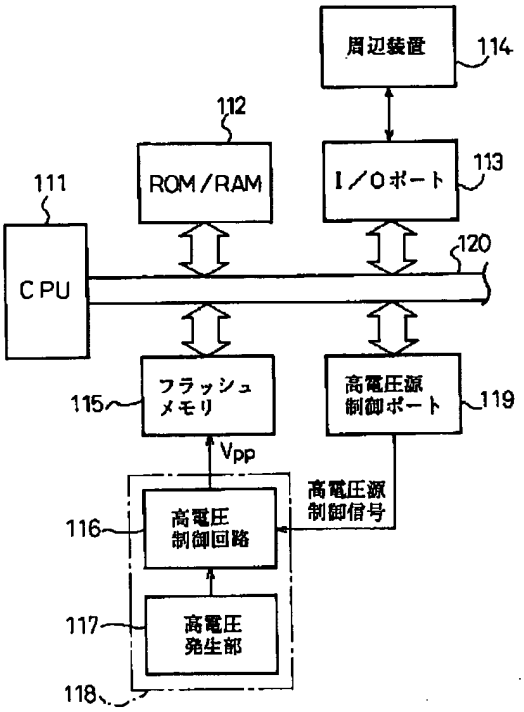


[Drawing 10]

DC－DCコンバータ内蔵フラッシュメモリの実施例

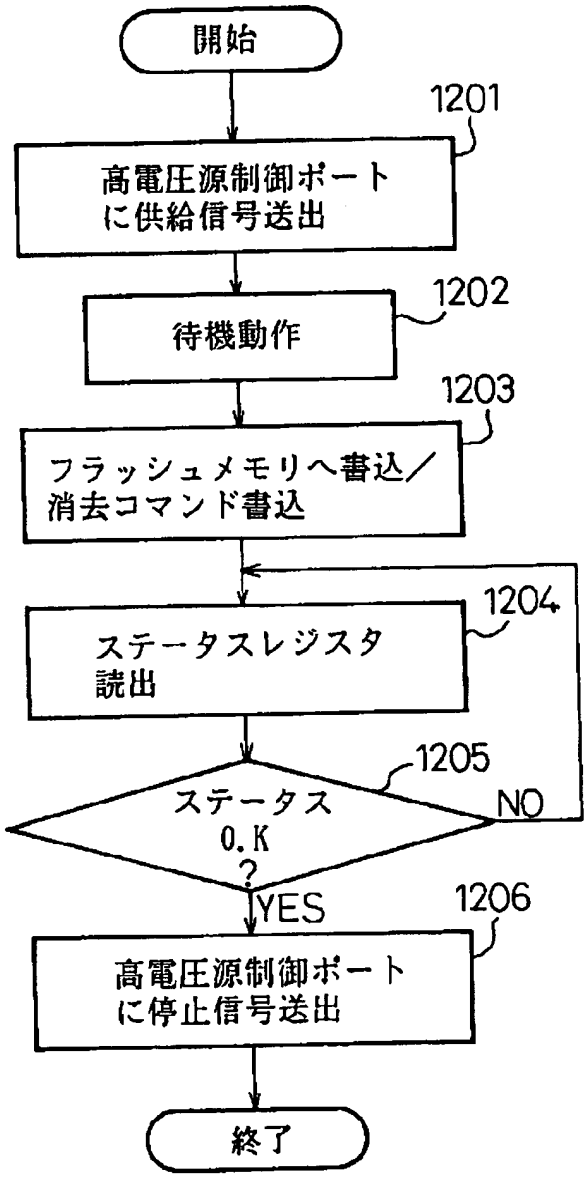


[Drawing 11]
従来のフラッシュメモリを用いたシステム構成例



[Drawing 12]

従来例のシステム制御動作



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